SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from prior Japanese Patent Application No. 2006-256194, filed Sep. 21, 2006, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor memory and a method of manufacturing the same.

[0004] 2. Description of the Related Art

[0005] Flash memories are widely used to store large-volume data in, e.g., cell phones, digital still cameras (DSCs), USB memories, and silicon audio, and the markets of these flash memories keep extending due to the reduction in manufacturing cost per bit (bit cost) resulting from rapid scaling of the device dimension. New applications are also rapidly rising. The result is a favorable cycle in which the rapid scaling-down and the reduction in manufacturing cost find new markets.

[0006] In particular, a NAND flash memory has achieved a practical cross-point cell by allowing a plurality of active areas (AAs) to share a gate electrode (GC), and its simple structure allows rapid progress of scaling. NAND flash memories are beginning to be widely used for storage purposes in, e.g., the USB memories and silicon audio described above, since the above-mentioned rapid scaling-down reduces the bit cost. Accordingly, the recent NAND flash memories are leading devices of LSI (Large Scale Integration) scaling, and the minimum half pitch has reached 0.1 μm or less even on the mass-production level. Although the technical difficulties are also abruptly increasing with the rapid scaling of the dimension, demands are arising for further scaling in the future.

[0007] Unfortunately, many problems must be solved to further scaling of flash memories. The problems are enumerated below:

[0008] (1) The development of lithography techniques cannot follow the rapid device scaling. Presently, mass-production of lithography apparatuses starts immediately after they are put on sale. In the future, therefore, it is necessary to increase the bit density while keeping the lithography techniques in status quo.

[0009] (2) Since the dimensions of elements decrease as micropatterning progresses, the short-channel effect or narrow-channel effect abruptly worsens. This makes it difficult to ensure the reliability and increase the operating speed of nonvolatile memories generation by generation.

[0010] (3) As scaling advances, the dimensions of elements decrease. Therefore, statistical variations in numbers of atoms of dopant impurities of transistors and the like presumably worsen the device characteristics or the variations in device characteristics in the future.

[0011] Accordingly, it is highly likely to become difficult to continuously increase the bit density in the future by simple scaling of elements size in the horizontal plane only.

[0012] The present inventor, therefore, has invented a stacked memory as a semiconductor memory structure capable of relatively easily increasing the bit density of memory elements, without entirely depending upon micropatterning of the lithography techniques, and a method of manufacturing the stacked memory.

[0013] As well-known examples of stacked memories, methods of sequentially stacking memory layers as described in patent references 1 to 8, and some stacked memories are presently mass-produced. However, any of these methods forms memory layers by stacking one layer at a time. If the number of memory layers increases, therefore, the number of manufacturing steps largely increases.

[0014] [Patent reference 1] Jpn. Pat. Appln. KOKAI Publication No. 7-235649

[0015] [Patent reference 2] U.S. Pat. No. 6,534,403B2

[0016] [Patent reference 3] United States Patent Application Publication Pub. No. US2005/0014334A1

[0017] [Patent reference 4] United States Patent Application Publication Pub. No. US2005/0012119A1

[0018] [Patent reference 5] United States Patent Application Publication Pub. No. US2005/0012120A1

[0019] [Patent reference 6] United States Patent Application Publication Pub. No. US2005/0012154A1

[0020] [Patent reference 7] United States Patent Application Publication Pub. No. US2005/0012220A1

[0021] [Patent reference 8] United States Patent Application Publication Pub. No. US2005/0014322A1

BRIEF SUMMARY OF THE INVENTION

[0022] A semiconductor memory according to the first aspect of the present invention comprises a plurality of stripe-like active areas formed by stacking, in a direction perpendicular to a substrate, a plurality of layers extending parallel to the substrate, a first gate electrode formed on first side surfaces of the active areas, the first side surfaces being perpendicular to the substrate, a second gate electrode formed on second side surfaces of the active areas, the second side surfaces being perpendicular to the substrate, and wherein the layers are patterned in self-alignment with each other, intersections of the active areas and the first gate electrode form a plurality of memory cells, and the plurality of memory cells in an intersecting plane share the first gate electrode.

[0023] A semiconductor memory manufacturing method according to the second aspect of the present invention comprises depositing a plurality of layers on a substrate, forming a plurality of stripe-like active areas by processing the layers in self-alignment with each other, and forming a plurality of gate electrodes intersecting the active areas in a longitudinal direction thereof, wherein each of the active areas uses, as a channel region, at least one of two side surfaces perpendicular to the substrate, intersections of the active areas and the gate electrodes form memory cells, and a plurality of memory cells in an intersecting plane share the gate electrode.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0024] FIG. **1** is a perspective view showing a main manufacturing step of a semiconductor memory according to the first embodiment of the present invention;

[0025] FIG. **2** is a sectional view showing a main manufacturing step of the semiconductor memory according to the first embodiment of the present invention;